Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**G**

**Top Material: Al**

**Backside Material: Ti Ni Ag**

**Bond Pad Size: G = .018” X .026” S = .041” X .061”**

**Backside Potential: Drain**

**Mask Ref: GEN III**

**APPROVED BY: DK DIE SIZE .162” X .219” DATE: 1/10/22**

**MFG: Vishay THICKNESS .016” P/N: IRFC9240**

**DG 10.1.2**

#### Rev B, 7/19/02